PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 39/24, 39/22, 39/00, 21/311, 21/3065, 21/467

A1

(11) International Publication Number: WO 00/16414

(43) International Publication Date: 23 March 2000 (23.03.00)

(21) International Application Number: PCT/AU99/00774

(22) International Filing Date: 14 September 1999 (14.09.99)

(30) Priority Data:
PP 5907 14 September 1998 (14.09.98) AU

(71) Applicant *(for all designated States except US)*: COMMONWEALTH SCIENTIFIC AND INDUSTRIAL RESEARCH ORGANISATION [AU/AU]; Limestone Avenue, Campbell, ACT 2601 (AU).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: FOLEY, Cathy [AU/AU]; Bradfield Road, West Lindfield, NSW 2070 (AU).

(74) Agent: F B RICE & CO; 605 Darling Street, Balmain, NSW 2041 (AU).

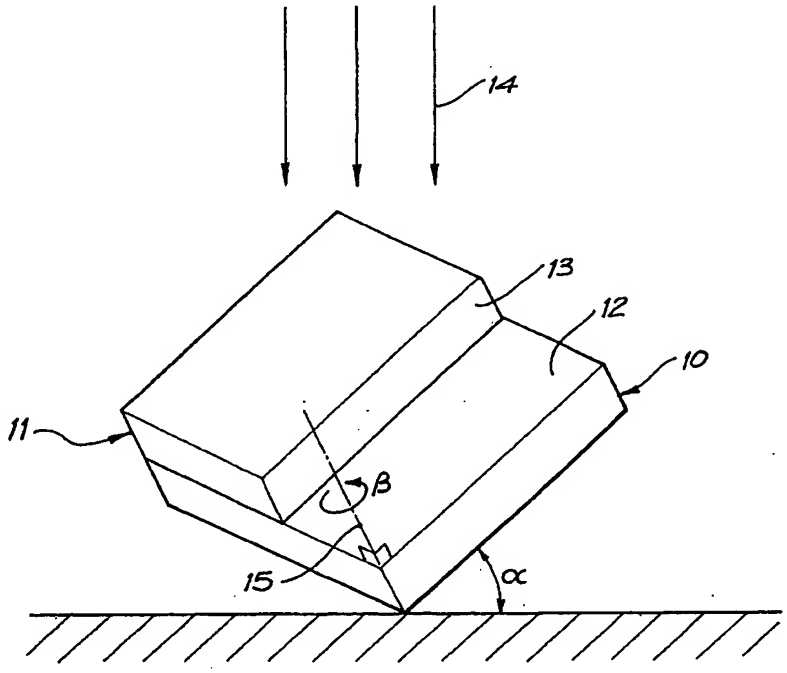
(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: METHOD OF FABRICATION OF STEP EDGE

(57) Abstract

A method of forming a step edge in a surface (12) of a crystalline substrate (10) is provided. The method includes forming a layer of resist (11) over the surface (12) and removing areas of the resist (11) to expose selected areas of the surface (12), thereby forming side walls (13) in the layer of the resist (11), the side walls (13) bounding the exposed areas of the surface (12). The method also includes exposing the resist (11) and substrate (10) to an ion beam (14), thereby etching the resist (11) and the exposed areas of the surface (12), and controlling the orientation and angle of incidence of the ion beam (14) with respect to the substrate (10) and the resist side walls (13) to form a step edge with desired angle and height characteristics. An angular position of the substrate (10) about an axis (15) formed by a normal to the surface (12) is controlled in order to control the step edge formation.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

"Method of fabrication of step edge"

Technical Field

The present invention relates to the construction of circuits including a substrate, and in particular provides a method of forming a step edge in a substrate.

Background Art

Superconducting materials are currently finding applications in a number of areas. For example, superconducting quantum interference devices (SQUIDs) have applications in geophysical mineral prospecting.

In many instances it is desired to form features in the surface of a substrate to alter or control physical or electrical aspects of circuits constructed over the substrate. For example, a 'step edge' in the surface of the substrate is commonly required in the construction of circuits.

A common circuit element in superconducting devices is the Josephson Junction, which may be formed in a variety of ways. Josephson Junctions are commonly implemented by forming the superconducting material over a step edge in a substrate. However, characteristics of the junction, such as the critical density, can be difficult to control.

Disclosure of Invention

Throughout the following, the terms 'superconducting material', 'superconducting device' and the like are used to refer to a material or device which, in a certain state and at a certain temperature, is capable of exhibiting superconductivity. The use of such terms does not imply that the material or device exhibits superconductivity in all states or at all temperatures.

From a first aspect the present invention provides a method of forming a step edge in a surface of a crystalline substrate, including the steps of:

forming a layer of resist over the surface;

removing areas of the resist to expose selected areas of the surface, thereby forming side walls in the layer of the resist, the side walls bounding the exposed areas of the surface; and

exposing the resist and substrate to an ion beam, thereby etching the resist and the exposed areas of the surface;

wherein the angles between an axis of incidence of the ion beam and the surface, and between the axis of incidence of the ion beam and the resist side walls, are selected in order to form a step edge with predetermined angle

and height characteristics, and wherein an angular position of the axis of incidence of the ion beam about an axis formed by a normal to the surface is selected in order to control the step edge formation.

The selection of the angular position of the axis of incidence of the ion beam about the axis formed by the normal to the surface may be made in order to control or alter an etch rate of the substrate, for example by controlling or altering an incidence of the ion beam relative to channels in a lattice of the crystalline substrate.

The resist side wall is preferably at an angle to the surface of the substrate of greater than 70 degrees, and even more preferably greater than 80 degrees. Most preferably, the resist side wall is substantially perpendicular to the surface of the substrate.

The angle of the resist side wall may be optimised by controlling the steps involved in formation of the layer of resist and the removal of areas of the resist, namely hot plate temperature, pre-exposure development, exposure time, UV light intensity, post exposure baking temperature and development time.

In embodiments where the angle of the step edge is desired to be large, the method of the invention may include the steps of:

orientating the ion beam such that the angle between the axis of incidence of the ion beam and a plane of the resist side wall is minimised, thereby minimising an etch rate of the resist side wall; and

altering the angle between the axis of incidence of the ion beam and the surface in order to control an etch rate of the substrate.

Alternative embodiments, in which the angle of the step edge is desired to be low, may include the steps of:

orientating the ion beam such that the angle between the axis of incidence of the ion beam and a plane of the resist side wall is sufficiently large to cause an etch rate of the resist side wall to be increased; and

altering the angle between the axis of incidence of the ion beam and the surface in order to control an etch rate of the substrate.

During a period of time in which the resist and substrate are exposed to the ion beam, both the substrate and the resist side wall will be etched by the ion beam. Consequently, the resist side wall will gradually recede from the exposed areas of the surface, thereby exposing further areas of the surface to the ion beam. The further areas of the substrate surface will be exposed to

the ion beam for a reduced amount of time, and therefore the substrate will be less deeply etched in these areas, forming the step edge of a certain angle.

The angle of the step edge may be controlled in order to obtain predetermined characteristics in a circuit subsequently constructed over the substrate. For example, a high temperature superconductor may later be formed over the substrate, with a Josephson junction being formed over the step edge. By forming a step edge having a predetermined angle, the critical current of the Josephson junction may, to some extent, be selected.

The substrate used in preferred embodiments of the invention is a single crystal MgO (100) substrate.

The step of removing areas of the resist is preferably performed by photolithography.

The resist and substrate are preferably exposed to an argon ion beam.

The method of the first aspect of the invention preferably includes the preliminary step of:

providing a smooth substrate surface, for example by polishing the surface of the substrate.

The substrate preferably has a surface roughness of less than 0.4nm.

The method of the first aspect of the invention preferably includes the subsequent steps of:

removing all of the resist; and

cleaning the surface of the substrate to smoothen irregularities in the surface and to remove any debris that may have been created during previous steps.

A height of the step edge may be influenced by controlling a time for which the surface and resist are exposed to the ion beam.

Preferably, the method of the first aspect of the invention provides a step edge suitable for forming a Josephson junction in a superconducting material, having a single grain boundary at the upper part of the step edge, and a rounded step base.

The superconducting material is preferably $YBa_2Cu_3O_x$ (YBCO), where x has a value of 6 to 7. YBCO is advantageous in the present method because it grows over an MgO substrate such that its c-axis remains substantially perpendicular to the underlying substrate, enabling grain boundaries to be created in the YBCO HTSC layer. Consequently, in cases where a Josephson junction is constructed over the step edge, the critical current of the junction

may be controlled by the angle of the step edge, and by the number of misorientation angles that are formed in the step.

Brief Description of Drawings

Embodiments of the invention will now be described by way of example with reference to the accompanying drawings in which:

Figure 1 shows a substrate being exposed to an ion beam in accordance with the first aspect of the present invention;

Figures 2 and 2a show views of the substrate of Figure 1 before and after etching;

Figures 3a to 3e are scanning electron micrographs of the morphology of step edges formed in accordance with the present invention;

Figure 4 illustrates the effect of simultaneous etching of the resist side wall and the substrate; and

Figures 5a to 5d are scanning electron micrographs of the morphology of step edges which have been cleaned by a final ion beam etch.

Modes for Carrying Out the Invention

In accordance with a first aspect of the present invention, Figure 1 shows a crystalline substrate 10 having a layer of resist 11 formed over a surface 12 of the substrate 10. Areas of the resist have been removed in order to expose an area of the surface 12, and the resist has a side wall 13 adjoining the exposed area of the surface 12. The substrate 10 and resist 12 are being exposed to an argon ion beam 14 of controlled orientation and angle of incidence with respect to the surface 12 and to the side wall 13, thereby etching the exposed areas of the surface 12 and the resist side wall 13 at controlled rates. Appropriate control of the orientation and angle of incidence of the ion beam 14 and the period of exposure, provides a step edge of desirable angle and height.

The present invention will now be described by way of example. We define α to be the angle of the substrate 10 to the ion beam 14, and β to be the angular position of the substrate 10 about an axis 15 formed by a normal to the plane of the surface 12.

As shown in Figure 2, resist side wall 13 is at an angle χ of between 80° and 85° to the surface 12. This angle is preferably as close as possible to 90°, and may be optimised by controlling the steps involved in formation of the

layer of resist 11 and the removal of areas of the resist, namely hot plate temperature, pre-exposure development, exposure time, UV light intensity, post exposure baking temperature and development time. Resist side walls at an angle of between 80° and 85° to surface 12 are routinely achieved in this way. The argon ion beam 14 forms an angle γ with the normal 16 of the plane of the resist side wall 13.

Substrate 10 is a MgO (100) substrate polished on one side, to have a surface roughness of better than 0.4nm. A 1.3μm photoresist mask 11 (Shipley S98913 - available from AWA Electronics, 8 Australia Ave, Homebush Bay, Sydney, Australia) is used to define the step edge. The argon ion beam is produced by a Kaufman ion gun providing a beam voltage of 500eV and a neutralised beam current of 22mA/cm^2 on a water cooled substrate holder.

In order to form a step edge of desired angle φ, the etching rate of the substrate 10 and the etching rate of the resist side wall 13 are controlled. Our measurements indicate that the etching rates of MgO (100) and Shipley S98913 photoresist vary with different incident angles, α. From normal incidence (α=0°), the etching rate increases until reaching a maximum at α=50° - 60°, then decreases as larger glancing angles are approached. The initial increase in rate occurs as a consequence of the increased probability of the Ar ion collisions giving a substrate atom a component of momentum directed away from the surface 12. The reduction in etching rate at higher angles occurs because the incoming ion beam is spread over an increasingly larger surface area (the flux drops off as the cosine of the incidence angle). Also, the probability of a purely elastic reflection of the primary beam is increased at large angles of incidence.

There follows an example of the effect of altering α, while keeping γ close to the glancing angle (>70°), thereby causing a slow etch rate of the resist side wall 13. The etching rate of the MgO (100) substrate 10 is increased by raising the ion beam 14 angle of incidence from zero up to 60° - 70°. Note that γ remains substantially constant as α is changed. Therefore the etch rate of the resist side walls 13 is constant, at a small value, and the etch rate of the MgO substrate 10 is altered. Consequently, it is possible to alter the ion milled surface step angle φ. Figure 3 shows scanning electron micrographs of the step edge morphology after the resist mask has been removed, for α varied from 30° to 70° in 10° increments. The steepness of the

step edge increases with α up to 60-70°. A 'rabbit ear' is observed on the top side of the step for α=60-70°, which is due to redeposited material backsputtered from the substrate surface. This material is mostly polycrystalline and would have a deleterious effect on subsequently grown layers such as YBCO, and so is preferably cleaned off (further described below).

In cases where a lower step edge angle φ is desired, γ may be reduced. This is now described by way of example. It is possible to fabricate a step edge with a moderate angle φ by aligning the substrate 10 so that the resist side wall 13 faces into the ion beam 14. Therefore the etch rate of the resist side wall 13 will be significant. With γ now being significantly less than 90 degrees, any change in α will affect γ. Specifically, increasing α will decrease γ. As shown in Figure 4, ion beam etching in such an orientation leads to the resist side wall 13 drawing back as shown by arrow 20 as it is etched away, simultaneously with the etching of the substrate 10 in the (100) direction as shown by arrow 21. The etch rate of the substrate 10 depends on α, whereas the etch rate of the resist side wall 13 depends on γ. Following etching, the resist and substrate will have drawn back, as shown by dotted line 22 in Figure 4.

The step angle φ may be influenced by altering the etch rate of the resist side wall with respect to the etch rate of the substrate. In accordance with the present invention, this may be achieved by altering β, thereby altering γ while maintaining a constant α. Moderate step angles φ are achieved when the etch rate for the substrate 10 is approximately equal to the etch rate for the resist side wall 13. The angles of α/γ = 50°/30°, 60°/20° or 70°/5° have been found to achieve a step angle of φ = 35°-40°. It has been noted that while an alteration of β does not change α, it does have a significant effect on the etch rate of the MgO crystalline substrate, but not on the etch rate of the resist, which may have an affect on the final result. For example if the etching rate of the MgO substrate 10 is too low, it may be possible to etch entirely through the photoresist and therefore etch and damage areas of the surface 12 which were not intended to be etched. If the etching rate of the MgO substrate 10 is too high, the resist side wall 13 may not draw back sufficiently to define a desired step angle.

This effect occurs because the etching rate increases at more oblique angles of incidence to a crystal structure, and material is more rapidly etched from side walls of channels formed by the crystal lattice structure.

As mentioned above, some substrate orientations lead to the formation of undesirable backsputtered debris on the surface 12, particularly near the top of the step edge. Such debris may cause unwanted misorientation angles in the step edge, for example causing increased junction noise in a Josephson junction subsequently constructed over the step edge. In preferred embodiments of the invention this debris is removed after creation of the step edge is complete and the resist has all been cleaned off the substrate. For example, the debris may be removed by a final ion beam etch, with the ion beam preferably being aligned perpendicular to the surface. Such a cleaning step may also improve the surface roughness, to provide a smoother mounting surface upon which circuits may subsequently be built. Step edges which have undergone an ion beam etch to remove debris and smoothen the surface are shown in Figure 5.

The present method enables production of a step edge having one, two or three junctions. In the preferred case, one junction is formed by making a step edge with a rounded bottom. The step edge may form two junctions by having a sharply defined edge at the top and bottom of the step. Alternatively, the present invention may provide a step edge having three junctions, wherein a 'trench' is formed along the bottom of the step, as indicated in Figure 3.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

CLAIMS:

1. A method of forming a step edge in a surface of a crystalline substrate, including the steps of:

forming a layer of resist over the surface;

removing areas of the resist to expose selected areas of the surface, thereby forming side walls in the layer of the resist, the side walls bounding the exposed areas of the surface; and

exposing the resist and substrate to an ion beam, thereby etching the resist and the exposed areas of the surface;

wherein the angles between an axis of incidence of the ion beam and the surface, and between the axis of incidence of the ion beam and the resist side walls, are selected in order to form a step edge with predetermined angle and height characteristics, and wherein an angular position of the axis of incidence of the ion beam about an axis formed by a normal to the surface is selected in order to control the step edge formation.

2. The method according to claim 1 wherein the selection of the angular position of the axis of incidence of the ion beam about the axis formed by the normal to the surface is made in order to control or alter an etch rate of the substrate, by controlling or altering an incidence of the ion beam relative to channels in a lattice of the crystalline substrate.

3. The method according to claim 1 or claim 2 wherein the resist side wall is at an angle to the surface of the substrate of greater than 70 degrees.

4. The method according to claim 3 wherein the resist side wall is at an angle to the surface of greater than 80 degrees.

5 The method according to claim 4 wherein the resist side wall is substantially perpendicular to the surface of the substrate.

6. The method according to any preceding claim wherein the angle of the resist side wall is controlled by controlling the steps involved in formation of the layer of resist and the removal of areas of the resist, namely hot plate temperature, pre-exposure development, exposure time, UV light intensity, post exposure baking temperature and development time.

7. The method according to any preceding claim wherein, in order to create a step edge of large angle, the method includes the further steps of:

orientating the ion beam such that the angle between the axis of incidence of the ion beam and a plane of the resist side wall is minimised, thereby minimising an etch rate of the resist side wall; and

altering the angle between the axis of incidence of the ion beam and the surface in order to control an etch rate of the substrate.

8. The method according to any one of claims 1 to 6 wherein, in order to create a step edge of low angle, the method includes the further steps of:

orientating the ion beam such that the angle between the axis of incidence of the ion beam and a plane of the resist side wall is sufficiently large to cause an etch rate of the resist side wall to be increased; and

altering the angle between the axis of incidence of the ion beam and the surface in order to control an etch rate of the substrate.

9. The method according to any one of claims 1 to 8 wherein the angle of the step edge is controlled in order to obtain predetermined characteristics in a circuit subsequently constructed over the substrate.

10. The method according to claim 9 wherein the circuit exhibits high temperature superconductivity.

11. The method according to claim 9 or 10 wherein a Josephson junction is formed over the step edge.

12. The method according to claim 11 wherein the critical current of the Josephson junction is controllably altered by altering the angle of the step edge.

13. The method according to any one of claims 1 to 12 wherein the substrate is a single crystal MgO (100) substrate.

14. The method according to any one of claims 1 to 13 wherein the step of removing areas of the resist is performed by photolithography.

15. The method according to any one of claims 1 to 14 wherein the resist and substrate are exposed to an argon ion beam.

16. The method according to any one of claims 1 to 15 wherein the method includes the preliminary step of:

providing a smooth substrate surface.

17. The method according to claim 16 wherein the smooth substrate surface is provided by polishing the surface of the substrate.

18. The method according to any one of claims 1 to 17 wherein the substrate has a surface roughness of less than 0.4nm.

19. The method according to any one of claims 1 to 18 wherein the method includes the subsequent steps of:

removing all of the resist; and

cleaning the surface of the substrate to smoothen irregularities in the surface and to remove any debris that may have been created during previous steps of the method.

20. The method according to any one of claims 1 to 19 wherein a height of the step edge is influenced by controlling a time for which the surface and resist are exposed to the ion beam.

21. The method according to any one of claims 1 to 20 wherein the method provides a step edge suitable for forming a Josephson junction in a superconducting material.

22. The method according to any one of claims 1 to 21 wherein the method provides a step edge suitable for forming a Josephson junction in a superconducting material, having a single grain boundary at the upper part of the step edge, and a rounded step base.

23. The method according to any one of claims 1 to 22 wherein a superconducting material which grows with its c-axis substantially perpendicular to the substrate is deposited over the substrate.

24. The method according to any one of claims 1 to 23 wherein YBa_2Cu_3Ox is deposited over the substrate, x being in the range of 6 to 7.

25. The method according to any one of claims 1 to 24 wherein a number of misorientation angles and the angle of the step edge control a critical current of a Josephson junction.

26. A superconducting device formed in accordance with the method of any preceding claim.

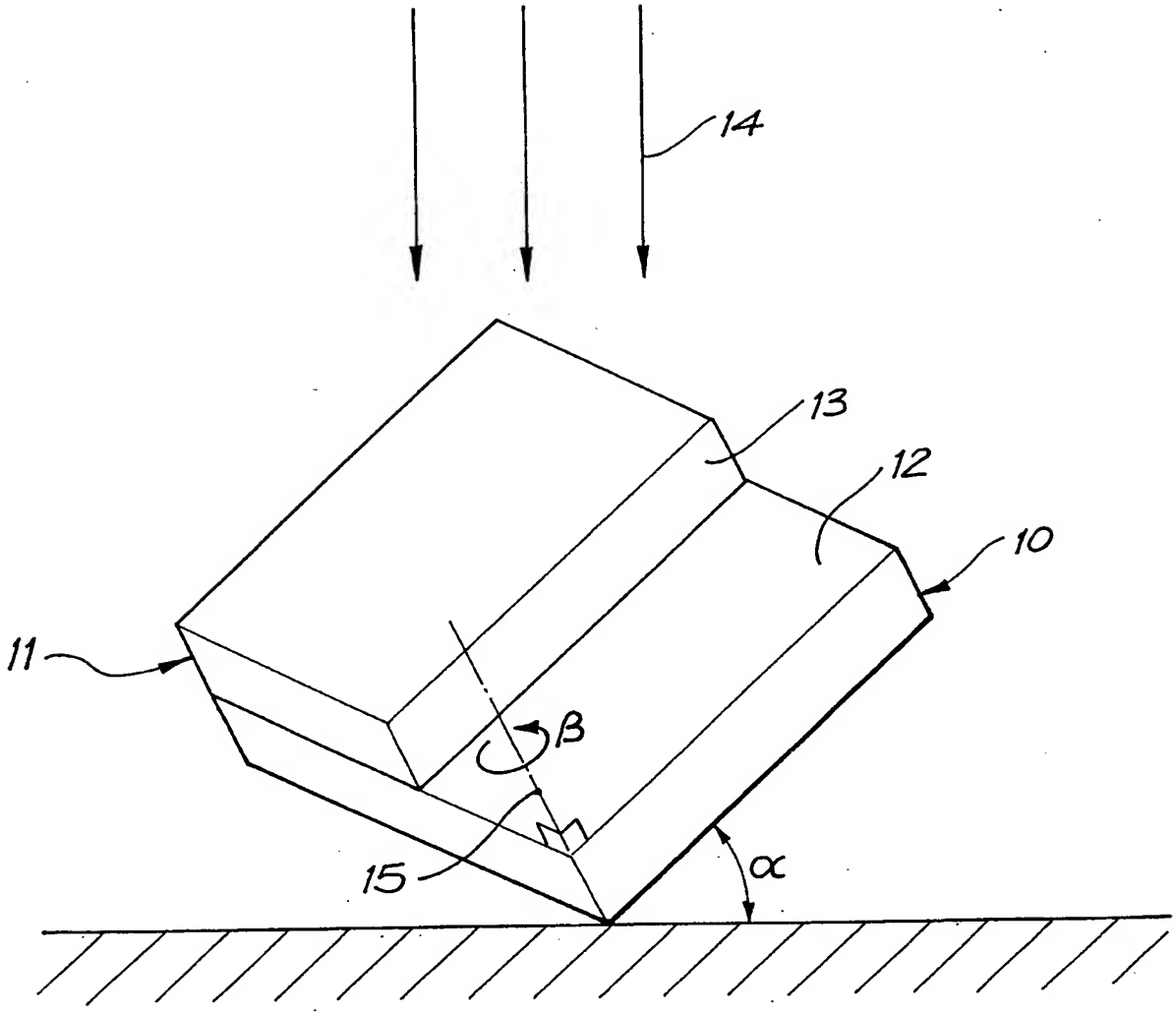


FIG. 1

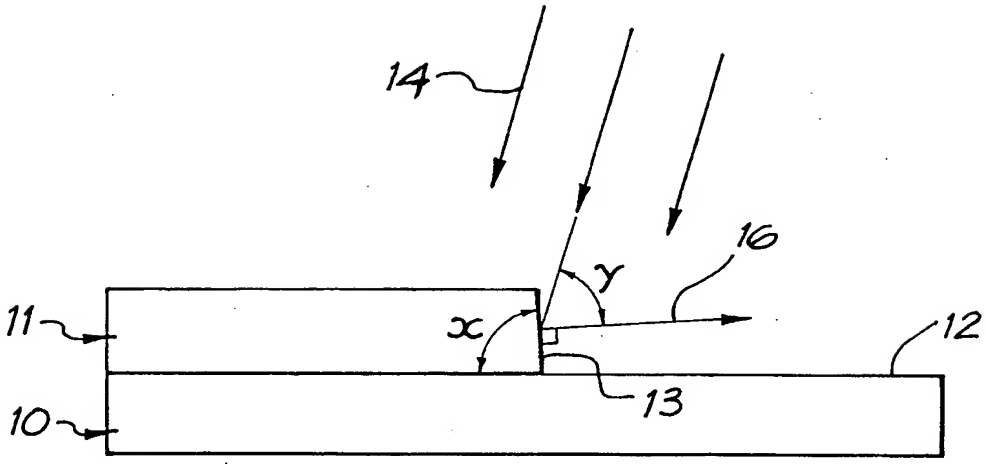


FIG. 2

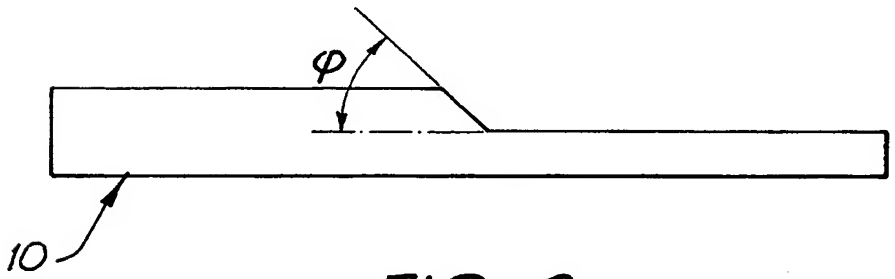
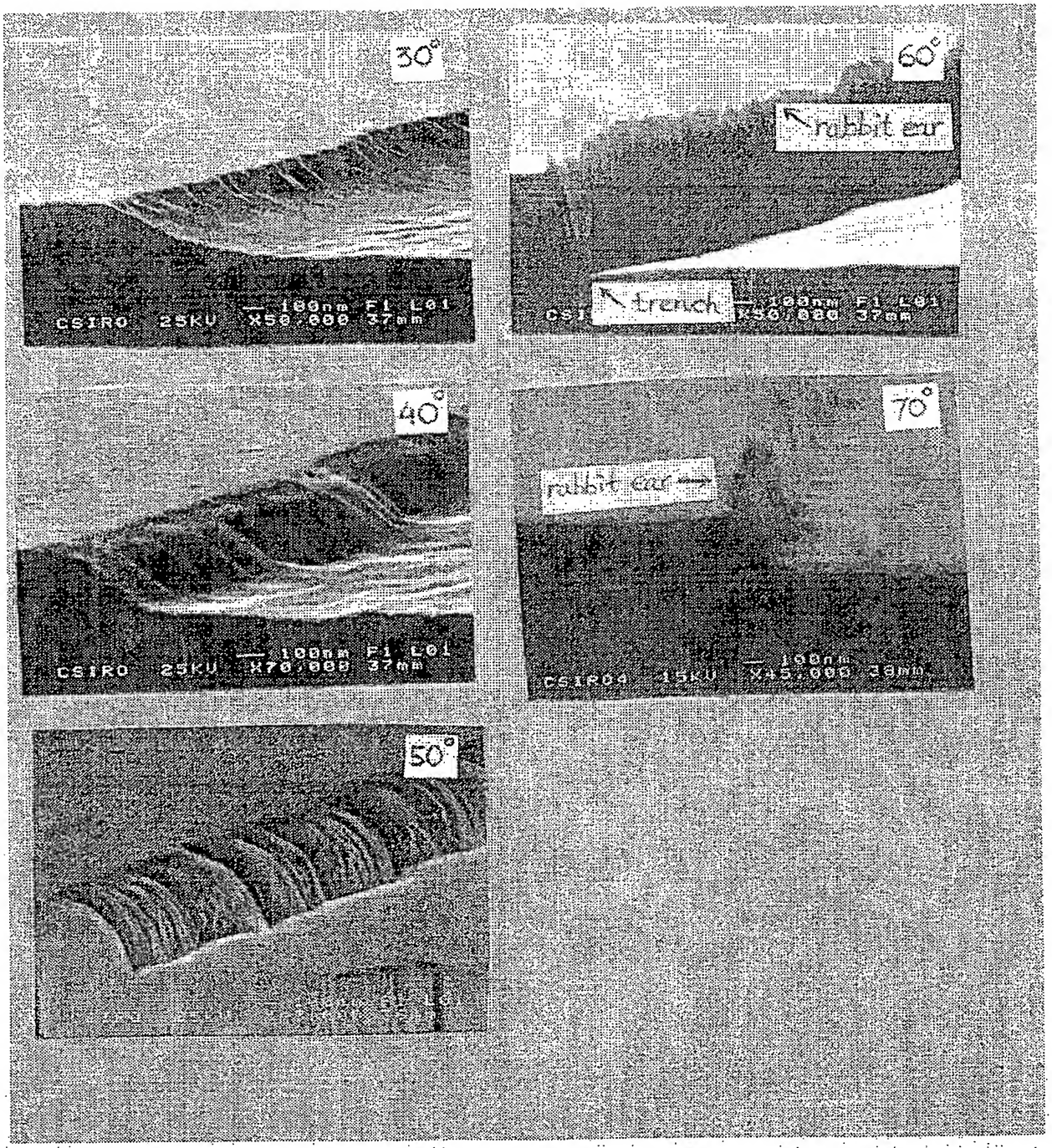


FIG. 2a

PCT/AU99/00774

Figure 3



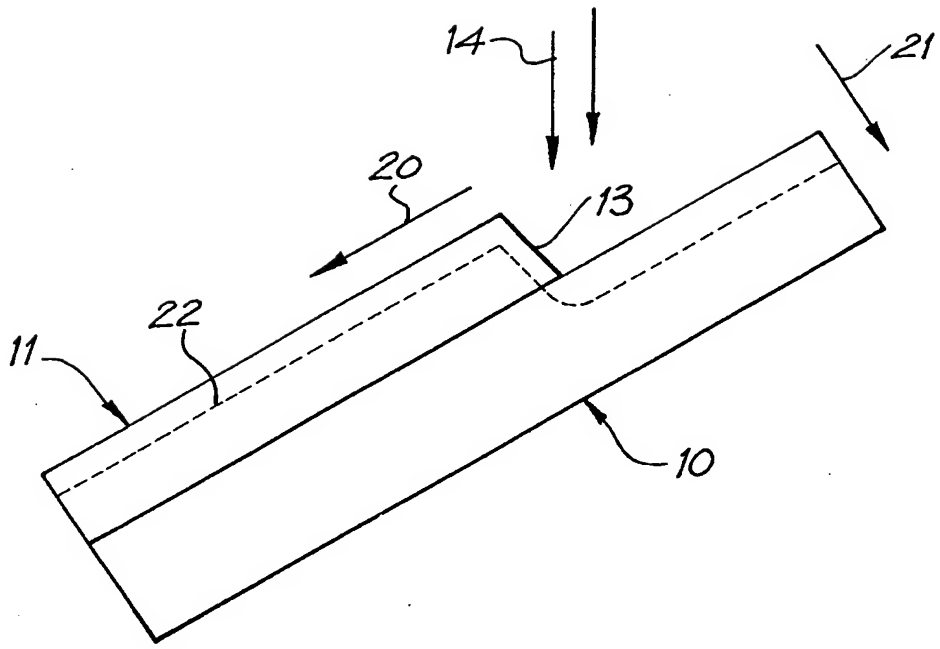


FIG. 4

Figure 5a

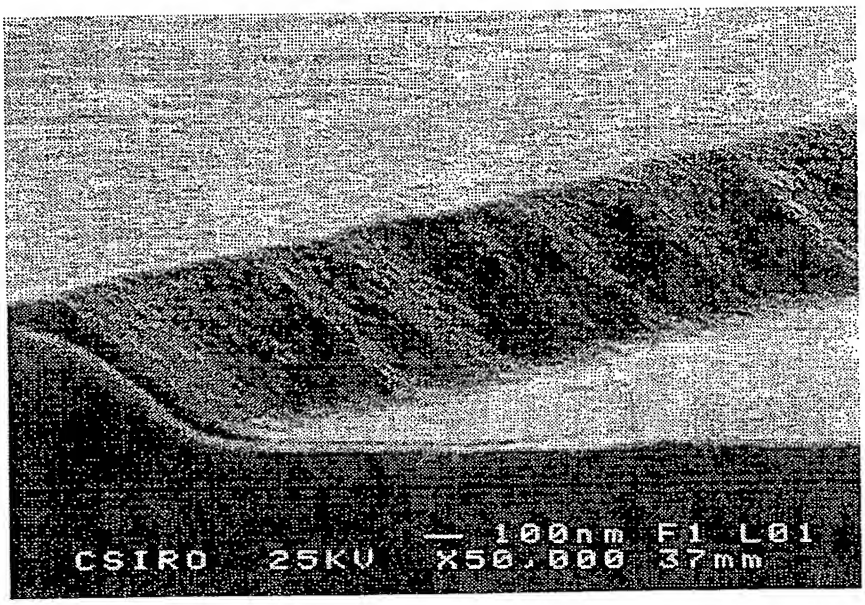


Figure 5b

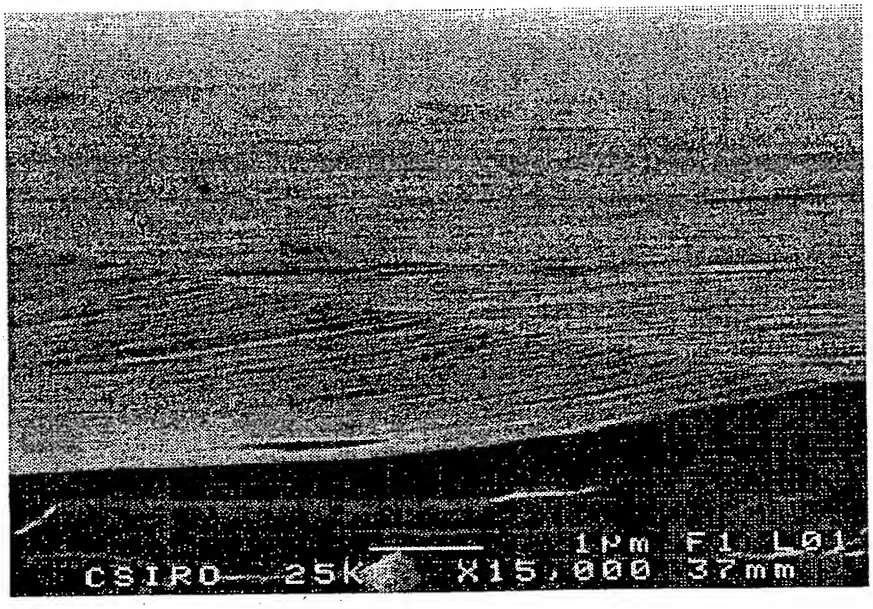


Figure 5c

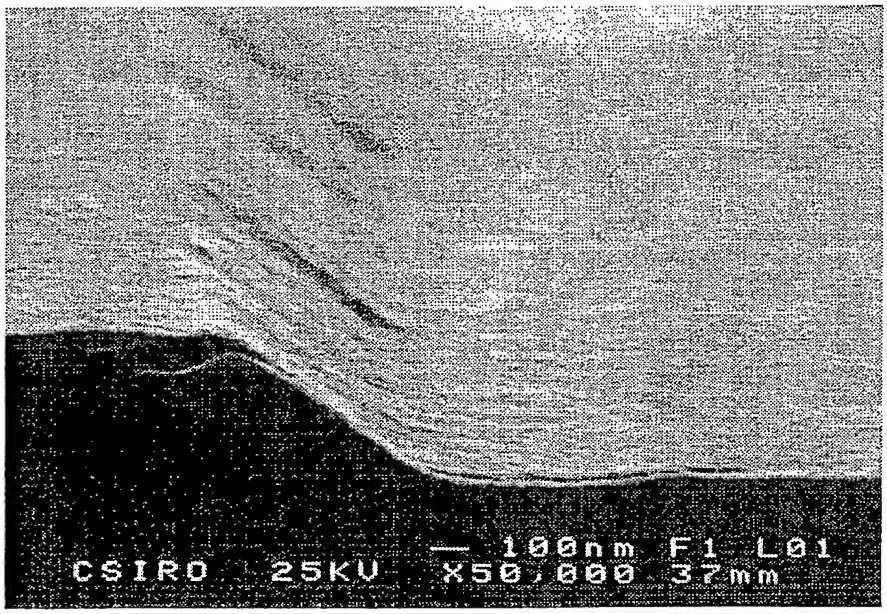
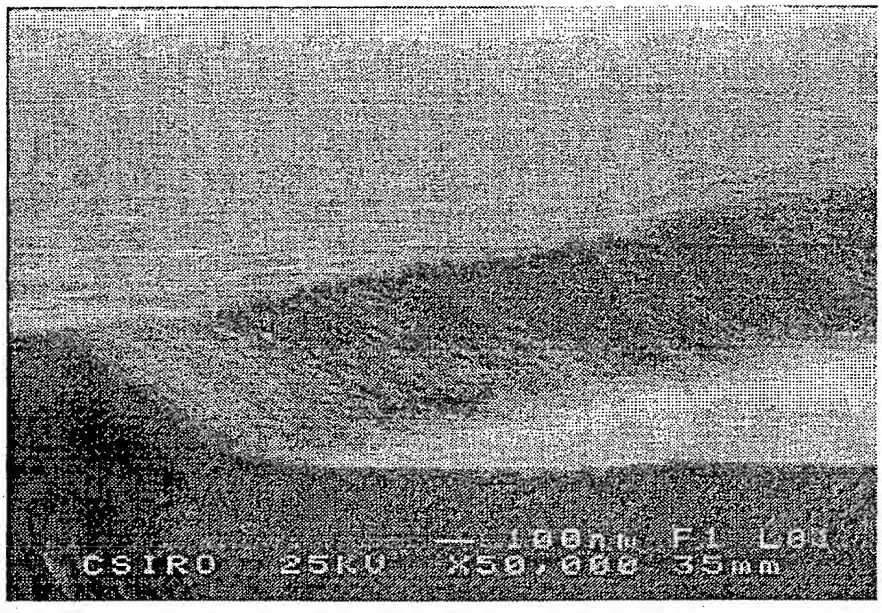


Figure 5d



INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 99/00774

A. CLASSIFICATION OF SUBJECT MATTER

Int Cl[6]: H01L 39/24, 39/22, 39/00, 21/311, 21/3065, 21/467

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
AU: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT: IPC as above with keywords: (STEP: or EDGE:) and ION and (ETCH: or REMOV:) and ((CRYSTAL
JAPIO: and (RESIST or PHOTORESIST)) or JOSEPHSON)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5358928 A (GINLEY et al.) 25 October 1994 column 4 line 17-29	
A	US 4966885 A (HEBARD) 30 October 1990 column 3 line 32-column 4 line 68	
A	EP 0660428 A (SUMITOMO ELECTRIC INDUSTRIES, LTD) 28 June 1995 page 4 line 25-page 6 line 8, Figure 1	

[X] Further documents are listed in the continuation of Box C

[X] See patent family annex

* Special categories of cited documents:

"A" Document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
05 November 1999	18 NOV 1999

Name and mailing address of the ISA/AU

AUSTRALIAN PATENT OFFICE
PO BOX 200
WODEN ACT 2606 AUSTRALIA
E-mail address: pct@ipaustralia.gov.au
Facsimile No.: (02) 6285 3929

Authorized officer

M.E. DIXON
Telephone No.: (02) 6283 2194

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 99/00774

C (Continuation). **DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Derwent Abstract Accession No: 94-262486/32, Class U11, U14, SE 9203489 A (TELEFONAKTIEBOLAGET ERICSSON, L M) 20 May 1994 abstract	
A	Derwent Abstract Accession No: 95-173951/23, Class L03, JP 07-094794 A (YUSEISHO TSUSHIN SOGO KENKYUSHO CHO) 7 April 1995 abstract	
A	IEEE Transactions on Applied Superconductivity, Volume 7, No: 2, June 1997 (ENSCHEDE, NETHERLANDS), D H A Blank et al., "Characterization of Ramp-type $YBa_2Cu_3O_7$ Junctions by AFM", pages 3323-3326 whole document	
A	Applied Physics Letters 63(15), 11 October 1993 (AMERICAN INSTITUTE OF PHYSICS), J Ramos et al., "$YBa_2Cu_3O_{7-\delta}$ Josephson junctions on directionally ion beam etched MgO substrates", pages 2141-2143 page 2141 column 1 line 31-column 2 line 1	
A	Applied Superconductivity, Volume 1, No: 10-12, issued 1993 (Jena, Germany), L Doerrer et al., "High T_c Thin Film Josephson Junctions and DC-SQUIDs", pages 1665-1673 page 1666 lines 14-24	

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/AU 99/00774

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
EP	660428	CA	2135500	FI	945234	JP	7079021
		US	5560836				

END OF ANNEX

Docket # W&B-INF-1908
Applic. #
Applicant: BERND GOEBEL ET AL.

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100 Fax: (954) 925-1101

DOCKET NO: _____
SERIAL NO: _____
APPLICANT: _____

LERNER AND GREENBERG P.A.
P.O. BOX 2480
HOLLYWOOD, FLORIDA 33022
TEL. (954) 925-1100